APPARATUS AND METHOD FOR AUTOMATED TRANSISTOR AND COMPONENT FOLDING TO PRODUCE CELL STRUCTURES

Abstract of the Disclosure

A method for generating an integrated circuit layout is disclosed. One embodiment includes receiving an integrated circuit netlist describing a plurality of transistors and a plurality of conductors for interconnecting the plurality of transistors, each of the plurality of transistors having a width in a layout corresponding to the integrated circuit netlist. More than one of the plurality of transistors are determined to be the widest transistors, all having the same width. One of the widest transistors is folded to produce a folded transistor that is electrically equivalent to the widest transistor. The folded transistor has at least two fingers, each finger having a smaller width than the width of the widest transistors. A fold solution for the layout having the one folded transistor is created.